Drill Table: Top Layer to Bottom Layer

	Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length	Drill Layer Pair	Tolerance
8	B	16	7.87mil (0.200mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+0/-7.874mil
8	C	74	8.00mil (0.203mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+0/-8mil
8	D	62	10.00mil (0.254mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+0/-10mil
8	E	510	12.20mil (0.310mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+0/-12.2mil
	G	6	23.62mil (0.600mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+/-3mil
	F	2	23.62mil (0.600mm)	PTH	Slot	51.18mil (1.300mm)	27.56mil (0.700mm)	Top Layer - Bottom Layer	+/-3mil
	H	2	33.47mil (0.850mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+/-3mil
	I	4	40.00mil (1.016mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+/-3mil
	J	6	40.16mil (1.020mm)	NPTH	Round	-	-	Top Layer - Bottom Layer	+/-2mil
	K	1	80.00mil (2.032mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+/-3mil
	L	8	118.11mil (3.000mm)	PTH	Round	-	-	Top Layer - Bottom Layer	+/-3mil
		691 Total							

Slot definitions : Rout Path Length = Calculated from tool start centre position to tool end centre position.
Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout

Drill Table: Layer 1 To Layer 2

8

LAYER STACK-UP :

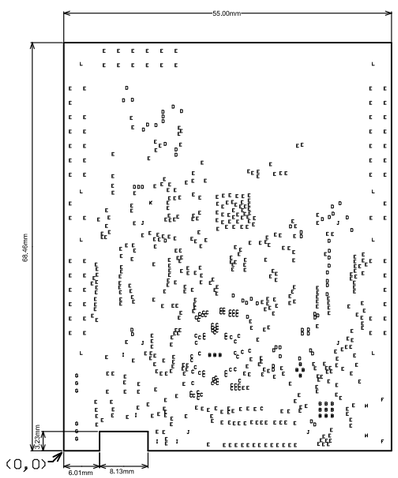
	Layer	Name	Material	Thickness	Constant	Board Layer Stack
	1	Top Overlay				
	2	Top Solder	Solder Resist	0.80mil	1	
6	3	Top Layer	Copper	1.60mil		
	4	Dielectric 1	RO4835 LOPRO	3.90mil	3.5	
	5	L2_GND	Copper	1.40mil		
	6	Dielectric 2	PCL370HR	5.50mil	4.17	
6	7	L3_SIGNAL 1	Copper	1.40mil		
	8	Dielectric 3	PCL370HR	10.00mil	4.17	
	9	L4_SIGNAL 2	Copper	1.40mil		
	10	Dielectric 4	PCL370HR	5.50mil	4.17	
	11	L5_SIGNAL 3	Copper	1.40mil		
	12	Dielectric 5	PCL370HR	10.00mil	4.17	
6	13	L6_SIGNAL 4	Copper	1.40mil		
	14	Dielectric 6	PCL370HR	5.50mil	4.17	
	15	L7_GND	Copper	1.40mil		
	16	Dielectric 7	PCL370HR	3.90mil	4.17	
6	17	Bottom Layer	Copper	1.60mil		
	18	Bottom Solder	Solder Resist	0.80mil	1	
	19	Bottom Overlay				

NOTE :
1. THIS IS AN IMPEDANCE CONTROLLED BOARD.
2. EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.

IMPEDANCE TABLE : 6

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	7.795 MILS	8 MILS	50 OHM	LAYER-2 (GND LAYER)

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP AND BOTTOM	5.2 MILS	5 MILS	100 OHM	LAYER-2 AND LAYER-7
L3 & L6	4.8 MILS	7.2 MIL	100 OHM	LAYER-2, LAYER 4 & LAYER-5, LAYER 7



NOTES:

1. VIA'S ON PAD AND BGA PACKAGE AREA SHOULD BE FILLED WITH CONDUCTIVE MATERIAL AND SURFACE SHOULD BE FLAT
   BGA AREA VIAS SHOULD BE CAPPED WITH COPPER PLATING TO ENSURE FLAT SURFACE
   FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON BOTH SIDES.
   OTHER THAN BGA AND VIA'S ON THE PAD VIA FILLING REQUIREMENT CAN BE EXMPTED
2. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.
3. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
4. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL.
5. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL.
6. REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3, 6 & 8.
7. FOR ACCURACY OF THE ANTENNA DIMENSION, NEED TO BE MEASURE THE ANTENNA DIMENSIONS ON ONE BAORD AS PER ANTENNA DOCUMENT(Visio-IWR_60GHz4).
8. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER.
9. INTENTIONAL ONE NET ANTENNA VIA IS PRESENT IN DESIGN.

1000.00mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 3.9 MIL
MIN. VIA PAD SIZE: 13.77 MIL
MINIMUM ANNULAR RING 0.0508mm (2.0MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER REFER STACK-UP
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER 57.37 MIL +/-10%
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[ ] MATTE [X] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 1 & 6 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: IWR6843ISK
DESIGNED FOR: Public Release
FILE NAME: PROC073C_PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC073	REV: C	SVN REV: Not In VersionControl
LAYER NAME = [illegible]	TID #: N/A		
PLOT NAME = Fabrication Drawing 1	GENERATED : 03-03-2020 14:20:55		TEXAS INSTRUMENTS

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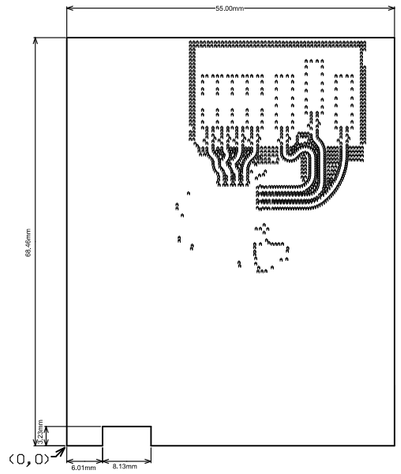
ENGINEER: Charles F. Oladimeji
LAYOUT BY: Tessolve
SCALE: 1.00
ALTIUM DESIGNER VERSION: 18.1.9.240

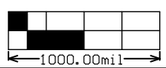
WO # : 308145-8143-D

Drill Table: Top Layer to Bottom Layer

Drill Table: Layer 1 To Layer 2

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length	Drill Layer Pair	Tolerance
A	981	5.90mil (0.150mm)	PTH	Round	-	-	Top Layer - L2_GND	+0/-5.9mil
	981 Total							





ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC073	REV: C	SVN REV: Not In VersionControl	
LAYER NAME = Board Dimensions	TID #: N/A			
PLOT NAME = Fabrication Drawing 2	GENERATED : 03-03-2020 14:20:56		TEXAS INSTRUMENTS	

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TEXAS INSTRUMENTS

PROJECT TITLE: IWR6843ISK

DESIGNED FOR: Public Release

FILE NAME: PROC073C_PCB.PcbDoc

ENGINEER: Charles F. Oladimeji

LAYOUT BY: Tessolve

SCALE: 1.00

ALTIUM DESIGNER VERSION: 18.1.9.240

WO # : 308145-8143-D